

# **APPARATUS AND METHOD FOR LARGE HARDWARE FINITE STATE MACHINE WITH EMBEDDED EQUIVALENCE CLASSES**

## **ABSTRACT OF THE DISCLOSURE**

[0047] A programmable finite state machine (FSM) includes, in part, first and second memories, and a selection circuit coupled to each of the memories. Upon receiving a  $(k+m)$ -bit word representative of the  $k$ -bit input symbol and the  $m$ -bit current state, the first memory supplies one or more matching transition rules stored therein. The selection circuit selects the most specific of the supplied rules. The transition rules are stored in the first memory in a ranking order of generality. The second memory receives the selected transition rule and supplies the next state of the FSM. The first memory may be a ternary content addressable memory and the second memory may be a static random access memory. The contents of both the content addressable memory and the static random memory is determined by an algorithm which minimizes the number of terms required to represent the next-state transition functions.

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